Specification Amendments

Please replace the paragraph bridging pages 41 and 42 with the following amended paragraph:

When a transistor arrangement of the type shown in FIGS. 14a and 14b is used for antifuse transistor 26, the hot carriers are generated at the inner portions of the split gate that are adjacent to the drain. Regardless of the particular geometry that is used for the antifuse, however, hot carrier generation is asymmetric -- more hot carriers are generated at one source-drain terminal (e.g., the drain) than are generated at the other source-drain terminal (e.g., the source). As a result, the portion of the gate oxide nearest the drain-source terminal that is injecting the hot carriers into the substrate (e.g., the gate oxide portion in the vicinity of the drain) is exposed to the highest concentration of hot carriers. By stressing the gate oxide asymmetrically -- i.e., by forcing the gate oxide to break down in the region in the vicinity of ~~the~~ a particular drain-source terminal rather than uniformly under the entire gate, the efficiency of the programming process is significantly enhanced.